**WHAT IS CLAIMED IS:**

1. A method for providing a phase-locked loop with reduced spurious tones, comprising:

comparing a reference clock signal to an internal clock signal to generate a first signal;

sampling the first signal based on a sampling clock signal to generate a second signal, the sampling clock signal reduced with respect to the reference clock signal; and

generating the internal clock signal based on the second signal.

2. The method of Claim 1, further comprising:

generating an up signal or a down signal based on the comparison of the reference clock signal to the internal clock signal;

generating a charge pump output signal based on the up and down signals;

generating the first signal based on the charge pump output signal;

generating an output frequency signal based on the second signal; and

dividing the output frequency signal by a predetermined amount to generate the internal clock signal.

3. The method of Claim 2, generating the charge pump output signal comprising sourcing current based on the up signal and sinking current based on the down signal, and generating the stabilized signal comprising injecting currents into a stabilization filter based on the up signal and draining currents from the stabilization filter based on the down signal.

4. The method of Claim 3, further comprising generating a loop filter output signal based on the second signal and generating the output frequency signal based on the second signal comprising generating the output frequency signal based on the loop filter output signal.

5. The method of Claim 1, further comprising:

dividing a reference frequency signal by a predetermined value, R, to generate the reference clock signal;

dividing the reference clock signal by a predetermined value, D, to generate a reduced frequency signal; and

generating the sampling clock signal based on the reduced frequency signal.

6. The method of Claim 5, generating the sampling clock signal based on the reduced frequency signal comprising creating a pulse based on the reduced frequency signal to generate a clock signal and buffering the pulse to generate an inverted clock signal.

7. The method of Claim 5, the predetermined amount comprising one of N and N+X/D.

8. A method for providing a phase-locked loop with reduced spurious tones, comprising:

dividing a reference clock signal by a predetermined value, D, to generate a reduced frequency signal;

generating a sampling clock signal based on the reduced frequency signal;

comparing the reference clock signal to an internal clock signal;

generating an up signal or a down signal based on the comparison of the reference clock signal to the internal clock signal;

generating a charge pump output signal based on the up and down signals;

generating a stabilized signal based on the charge pump output signal;

sampling the stabilized signal based on the sampling clock signal to generate a sampled output signal;

generating an output frequency signal based on the sampled output signal; and

dividing the output frequency signal by a predetermined amount to generate the internal clock signal.

9. The method of Claim 8, further comprising dividing a reference frequency signal by a predetermined value, R, to generate the reference clock signal.

10. The method of Claim 9, the predetermined amount comprising one of N and N+X/D, D comprising about 15, N comprising about 800, and R comprising about 10.

11. The method of Claim 8, generating the sampling clock signal based on the reduced frequency signal comprising creating a pulse based on the reduced frequency signal to generate a clock signal and buffering the pulse to generate an inverted clock signal.

12. The method of Claim 8, generating the charge pump output signal comprising sourcing current based on the up signal and sinking current based on the down signal.

13. The method of Claim 8, generating the stabilized signal comprising injecting currents into a stabilization filter based on the up signal and draining currents from the stabilization filter based on the down signal.

14. The method of Claim 8, further comprising generating a loop filter output signal based on the sampled output signal, generating the output frequency signal based on the sampled output signal comprising generating the output frequency signal based on the loop filter output signal.

15. A phase-locked loop, comprising:

a spur reduction circuit operable to receive a reference clock signal and to divide the reference clock signal by a predetermined value, D, to generate a reduced frequency signal;

a clock/buffer circuit coupled to the spur reduction circuit, the clock/buffer circuit operable to generate a sampling clock signal based on the reduced frequency signal;

a phase detector operable to compare the reference clock signal to an internal clock signal to generate an up signal or a down signal;

a charge pump coupled to the phase detector, the charge pump operable to generate a charge pump output signal based on the up and down signals;

a stabilization filter coupled to the charge pump, the stabilization filter operable to generate a stabilized signal based on the charge pump output signal;

a sampling circuit coupled to the stabilization filter and to the clock/buffer circuit, the sampling circuit operable to sample the stabilized signal based on the sampling clock signal to generate a sampled output signal;

an oscillator coupled to the sampling circuit, the oscillator operable to generate an output frequency signal based on the sampled output signal; and

a feedback divider coupled between the oscillator and the phase detector, the feedback divider operable to divide the output frequency signal by a predetermined amount to generate the internal clock signal.

16. The phase-locked loop of Claim 15, further comprising an input divider coupled to the phase detector and to the spur reduction circuit, the input divider operable to divide a reference frequency signal by a predetermined value, R, to generate the reference clock signal.

17. The phase-locked loop of Claim 16, the predetermined amount comprising one of N and N+X/D, D comprising about 15, N comprising about 800, and R comprising about 10.

18. The phase-locked loop of Claim 15, the clock/buffer circuit operable to generate the sampling clock signal by creating a pulse based on the reduced frequency signal to generate a clock signal, inverting the pulse to generate an inverted clock signal, and buffering the clock signal and the inverted clock signal.

19. The phase-locked loop of Claim 18, the sampling circuit comprising an n-channel transistor, a p-channel transistor and a hold capacitor, the n-channel transistor comprising a gate operable to receive the clock signal and the p-channel transistor comprising a gate operable to receive the inverted clock signal.

20. The phase-locked loop of Claim 15, further comprising a low pass filter coupled between the sampling circuit and the oscillator, the low pass filter operable to generate a loop filter output signal based on the sampled output signal, the oscillator operable to generate the output frequency signal based on the loop filter output signal.